



Shaarav Singh Gunsi

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B.Tech. in Computer Science and Engineering

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ACADEMIC DETAILS

Institute	Degree / Board	GPA / Marks(%)	Year
Indian Institute of Technology Delhi	B.Tech in CSE	9.56	2028
Maa Bharti Sr. Secondary School	CBSE(XII)	96.2	2024
NPS Indiranagar	CBSE(X)	96.8	2022

SCHOLASTIC ACHIEVEMENTS

- Incoming Quant Research/Quant Trading intern at Optiver's Sydney office (Summer 2027)
- Qualified for IOAA OCSC, India's Astronomy Olympiad camp, among the top 30 students selected nationwide
- Qualified for IICPC Codefest 2026 Regionals, securing Rank 259 after advancing from a prelims field of 13,800+ participants
- Qualified for IICPC Quantfest 2026 Regionals with a rank of 367 in Prelims, followed by a rank of 282 in Regionals.
- Top 1% national rank in: NSEA (Astronomy olympiad) 2023-2024, NSEC (Chemistry) 2024, and NSEP (Physics) 2024
- Advanced to the second level in Chemistry (INChO 2024) and Astronomy (INAO 2024) olympiads, among the top 300
- Awarded the Merit Prize in each of the first three semesters at IITD for academic performance in the top 7% of the batch
- Ranked 23rd among 461 teams in IIT Pokerbots 2026, organized by IIT Madras and sponsored by Jane Street
- Selected among the top 12 teams from IIT Delhi in QRT's Quant Challenge 2026 to advance to second round
- Department Rank 10 amongst 112 students in Computer Science and Engineering batch of 2028
- Was selected for Optiver's Future Focus program 2026 amongst around 150 students nationally, an intensive 5 day program into trading and research. Learnt trading terms and strategies, built algorithms and volatility models.
- Was selected for Meet Millennium 2026, Millennium's bootcamp, among 15 other students from over the country, for a two-day session about Millennium, AI, and other specifics on what it does, along with pre-intern interviews.
- Was invited to Mumbai for Da Vinci's Career Match event, a brunch where 10 of us were invited to talk to traders and quant devs from Da Vinci's Mumbai office, as well as a Group Discussion and pre-campus intern interviews.

PROJECTS

- **FPGA Programming in Verilog** / Prof. Preeti Ranjan Panda (July, 2025 - November, 2025):
 - Wrote a highway racing video game in Verilog, complete with a custom VGA driver for display, drawing pixels onscreen from ROM files, clock logic, control FSM, background movement, and switch-based car control. Implemented vector dot product computation: storing and manipulating vectors in BRAM blocks for memory optimization, and sequential multiplication logic. Also implemented linked lists and traversal, insertion and deletion operations. All these mini-projects were implemented on a Basys3 FPGA board, development done in Vivado.
- **DSA Projects** / Prof. Rohit Vaish (September, 2025 - November, 2025):
 - Developed a Git-like in-memory file system and a social network backend, implementing custom AVL trees, heaps, hash maps, and graph structures to support versioning, recommendations, and low-latency queries.
- **Sudoku Solver using Z3 & OCaml** / Prof. Sanjiva Prasad (Jan, 2026):
 - Built an end-to-end OCaml pipeline for encoding Sudoku instances as SAT constraints, interfacing with Z3, and reconstructing solved grids. Implemented solution-space analysis to classify puzzles as uniquely solvable, multiply solvable, or unsatisfiable.
- **Programming Languages assignments** / Prof. Sanjiva Prasad (Jan, 2026 - May, 2026):
 - Implemented a lexer and parser for a Lisp-like language using OCamllex and OCaml yacc. Built evaluators for the λ -calculus based on the Krivine and SECD abstract machines, and developed a stack-based interpreter for combinatory logic, exploring parsing, operational semantics, and functional language execution models.
- **Out-of-Order RISC-V Processor Simulator (C++)** / Prof. Rijurekha Sen (April, 2026):
 - Built a configurable cycle-level simulator for a 32-bit RISC-V processor implementing Tomasulo's algorithm, including reservation stations, register alias tables, reorder buffers, branch prediction, speculative execution, and precise exceptions. Modeled pipelined execution units, memory dependence handling via a load-store queue, and in-order retirement of architectural state.
- **Analytical Query Processing Engine (C++, Apache Arrow)** / Prof. Smruti Sarangi (May, 2026):
 - Developed a Pandas/Polars-inspired dataframe library supporting joins, aggregations, filtering, sorting, expression evaluation, and CSV/Parquet processing. Implemented lazy execution through DAG-based query planning and a rule-based optimizer featuring predicate/projection pushdown, constant folding, and expression simplification.

INTERNSHIPS

- **Summer Undergraduate Research Award (SURA) Internship** / Prof. Rajendra Kumar (May, 2026 - July, 2026)
 - Research Intern, Lattice-based Post-Quantum Cryptography: Investigated the complexity of Sparse-SIS and its relationship to SIS, developed hardness results and attack strategies for sparse lattice instances. Studied the impact of sparsity constraints on security guarantees, approximation factors, and cryptographic efficiency.

TECHNICAL SKILLS

- Python, C++, Verilog, RISC-V, Typescript, basic understanding of machine learning, quant finance, cryptography and probability